74LV244

Octal buffer/line driver (3-state)

Rev. 3 — 11 March 2014 Product data sheet

1. General description

The 74LV244 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC244 and 74HCT244.

The 74LV244 is an octal non-inverting buffer/line driver with 3-state outputs. The output enable inputs $1\overline{OE}$ and $2\overline{OE}$ control the 3-state outputs. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. The 74LV244 is identical to the 74LV240 but has non-inverting outputs.

2. Features and benefits

- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V; T_{amb} = 25 °C
- Typical V_{OHV} (V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V; T_{amb} = 25 °C
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV244N	−40 °C to +125 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74LV244D	−40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LV244DB	−40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74LV244PW	−40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4. Block diagram

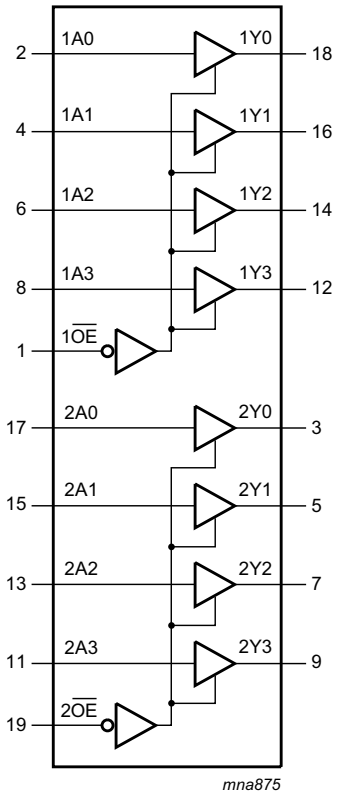


Fig 1. Functional diagram

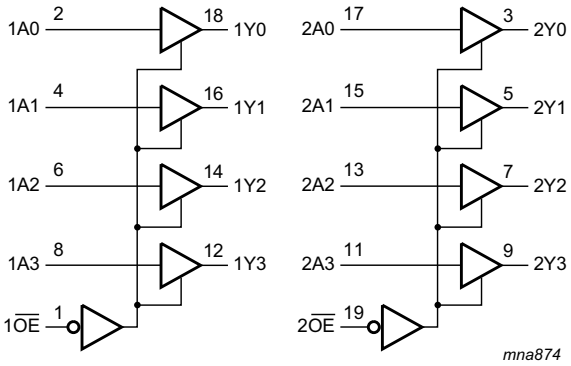


Fig 2. Logic symbol

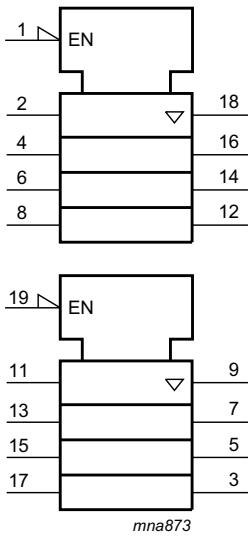


Fig 3. IEC logic symbol

5. Pinning information

5.1 Pinning

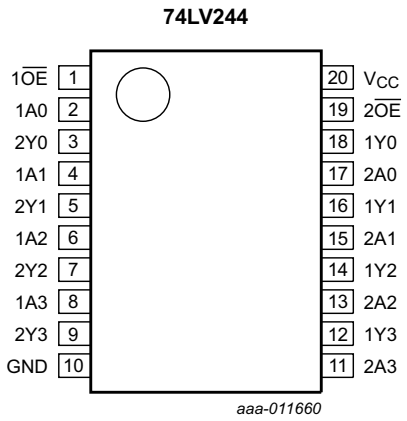


Fig 4. Pin configuration DIP20, SO20, SSOP20 and TSSOP20

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{OE}$, $2\overline{OE}$	1, 19	output enable input (active LOW)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	data input
2Y0, 2Y1, 2Y2, 2Y3	3, 5, 7, 9	bus output
GND	10	ground (0 V)
2A0, 2A1, 2A2, 2A3	17, 15, 13, 11	data input
1Y0, 1Y1, 1Y2, 1Y3	18, 16, 14, 12	bus output
V_{CC}	20	supply voltage

6. Functional description

Table 3. Function table[1]

Input		Output
$n\overline{OE}$	**nAn**	**nYn**
L	L	L
L	H	H
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±50	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V	-	±35	mA
I_{CC}	supply current		-	70	mA
I_{GND}	ground current		−70	-	mA
T_{stg}	storage temperature		−65	+150	°C
P_{tot}	total power dissipation	T_{amb} = −40 °C to +125 °C			
		DIP20 package [1]	-	750	mW
		SO20 [2]	-	500	mW
		SSOP20 and TSSOP20 [3]	-	400	mW

[1] For DIP20 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO20 packages: P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] For SSOP20 and TSSOP20 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	[1]	1.0	3.3	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		−40	-	+85	°C
			−40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.0 V to 2.0 V	0	-	500	ns/V
		V_{CC} = 2.0 V to 2.7 V	0	-	200	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	-	100	ns/V
		V_{CC} = 3.6 V to 5.5 V	0	-	50	ns/V

[1] The LV is guaranteed to function down to V_{CC} = 1.0 V (input levels GND or V_{CC}). DC characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 5.5 V.

9. Static characteristics

Table 6. Static characteristics

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH level input voltage	V_{CC} = 1.2 V	0.9	-	-	0.9		V
		V_{CC} = 2.0 V	1.4	-	-	1.4		V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0		V
		V_{CC} = 4.5 V to 5.5 V	$0.7V_{CC}$	-	-	$0.7V_{CC}$		V
V_{IL}	LOW level input voltage	V_{CC} = 1.2 V	-	-	0.3		0.3	V
		V_{CC} = 2.0 V	-	-	0.6		0.6	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8		0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	$0.3V_{CC}$		$0.3V_{CC}$	V
V_{OH}	HIGH level output voltage	$V_I = V_{IH}$ or V_{IL}; I_O = –100 µA						
		V_{CC} = 1.2 V	-	1.2	-	-	-	V
		V_{CC} = 2.0 V	1.8	2.0	-	1.8	-	V
		V_{CC} = 2.7 V	2.5	2.7	-	2.5	-	V
		V_{CC} = 3.0 V	2.8	3.0	-	2.8	-	V
		V_{CC} = 4.5 V	4.3	4.5	-	4.3	-	V
		$V_I = V_{IH}$ or V_{IL}						
		V_{CC} = 3.0 V; I_O = –8 mA	2.40	2.82	-	2.20	-	V
		V_{CC} = 4.5 V; I_O = –16 mA	3.60	4.20	-	3.50	-	V
V_{OL}	LOW level output voltage	$V_I = V_{IH}$ or V_{IL}; I_O = 100 µA						
		V_{CC} = 1.2 V	-	0	-	-	-	V
		V_{CC} = 2.0 V	-	0	0.2	-	0.2	V
		V_{CC} = 2.7 V	-	0	0.2	-	0.2	V
		V_{CC} = 3.0 V	-	0	0.2	-	0.2	V
		V_{CC} = 4.5 V	-	0	0.2	-	0.2	V
		V_{CC} = 3.0 V; I_O = 8 mA	-	0.25	0.40	-	0.50	V
		V_{CC} = 4.5 V; I_O = 16 mA	-	0.35	0.55	-	0.65	V
I_I	input leakage current	V_{CC} = 5.5 V; $V_I = V_{CC}$ or GND	-	-	1.0	-	1.0	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6 V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND	-	-	5	-	10	µA
I_{CC}	supply current	V_{CC} = 5.5 V; $V_I = V_{CC}$ or GND; I_O = 0 A	-	-	20	-	160	µA
ΔI_{CC}	additional supply current	per input; V_{CC} = 2.7 V to 3.6 V; $V_I = V_{CC}$ – 0.6 V	-	-	500	-	850	µA
C_I	input capacitance		-	3.5	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V); for test circuit, see Figure 7

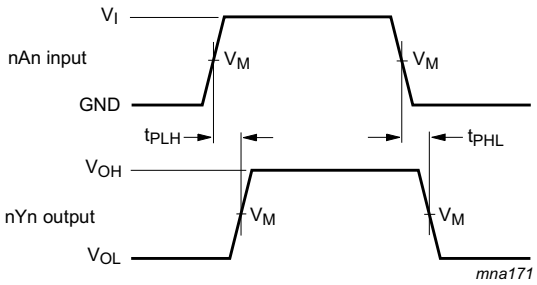
Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	1An to 1Yn; 2An to 2Yn; see Figure 5 [2]						
		V_{CC} = 1.2 V	-	50		-	-	ns
		V_{CC} = 2.0 V	-	17	24	-	31	ns
		V_{CC} = 2.7 V	-	13	17	-	23	ns
		V_{CC} = 3.0 V to 3.6 V	-	9	14	-	18	ns
		V_{CC} = 3.3 V; C_L = 15 pF	-	8.0	-	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	-	-	12	-	15	ns
t_{en}	enable time	$1\overline{OE}$ to 1Yn; $2\overline{OE}$ to 2Yn; see Figure 6 [2]						
		V_{CC} = 1.2 V	-	65	-	-	-	ns
		V_{CC} = 2.0 V	-	22	39	-	49	ns
		V_{CC} = 2.7 V	-	16	29	-	36	ns
		V_{CC} = 3.0 V to 3.6 V	-	12	23	-	29	ns
		V_{CC} = 4.5 V to 5.5 V	-	-	19	-	24	ns
t_{dis}	disable time	$1\overline{OE}$ to 1Yn; $2\overline{OE}$ to 2Yn; see Figure 6 [2]						
		V_{CC} = 1.2 V	-	60		-	-	ns
		V_{CC} = 2.0 V	-	22	34	-	43	ns
		V_{CC} = 2.7 V	-	17	24	-	32	ns
		V_{CC} = 3.0 V to 3.6 V	-	13	21	-	26	ns
		V_{CC} = 4.5 V to 5.5 V	-	-	16	-	19	ns
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}; V_{CC} = 3.3 V [3]	-	35	-	-	-	ns

[1] Unless otherwise stated, all typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] C_{PD} is used to determine the dynamic power dissipation $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ (P_D in µW), where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V.

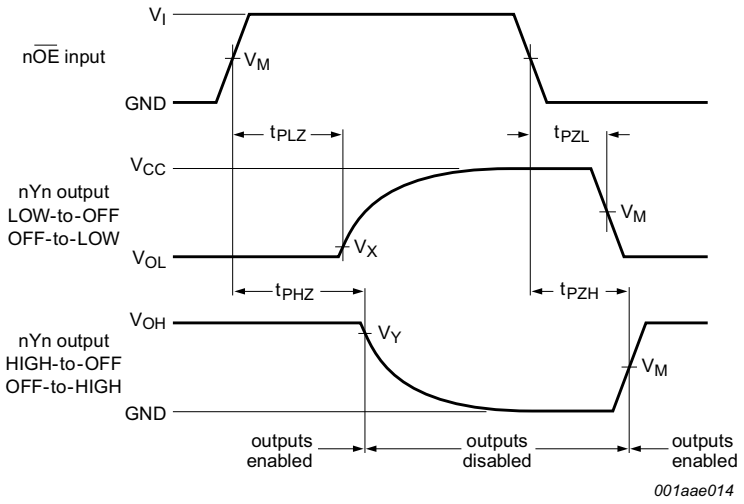
11. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. Input (nAn) to output (nYn) propagation delays



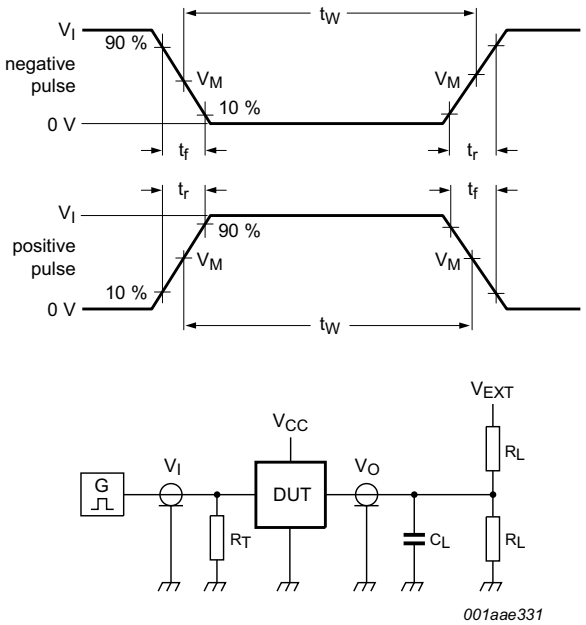
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. 3-state enable and disable times

Table 8. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V
≥ 4.5 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$



Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

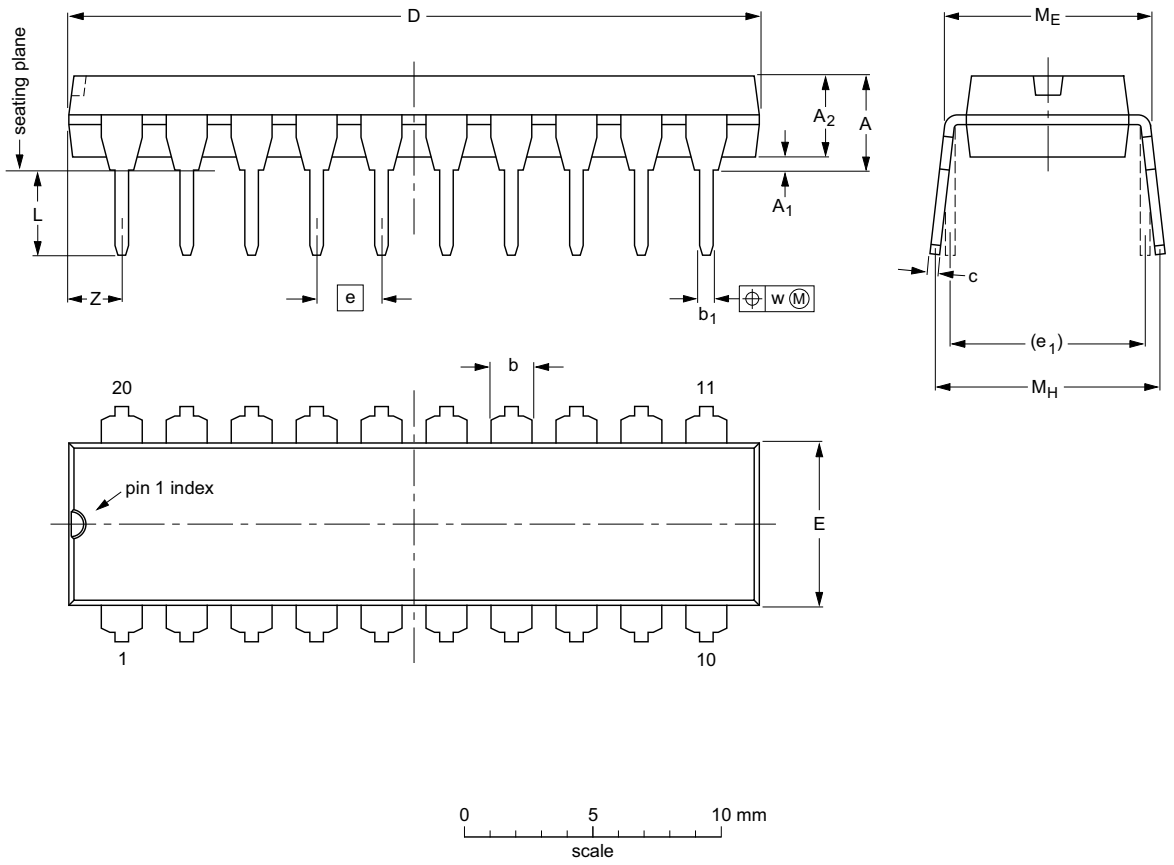
Fig 7. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
< 2.7 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	open	GND	$2V_{CC}$
2.7 V to 3.6 V	2.7 V	≤ 2.5 ns	15 pF, 50 pF	1 kΩ	open	GND	$2V_{CC}$
≥ 4.5 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	open	GND	$2V_{CC}$

12. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

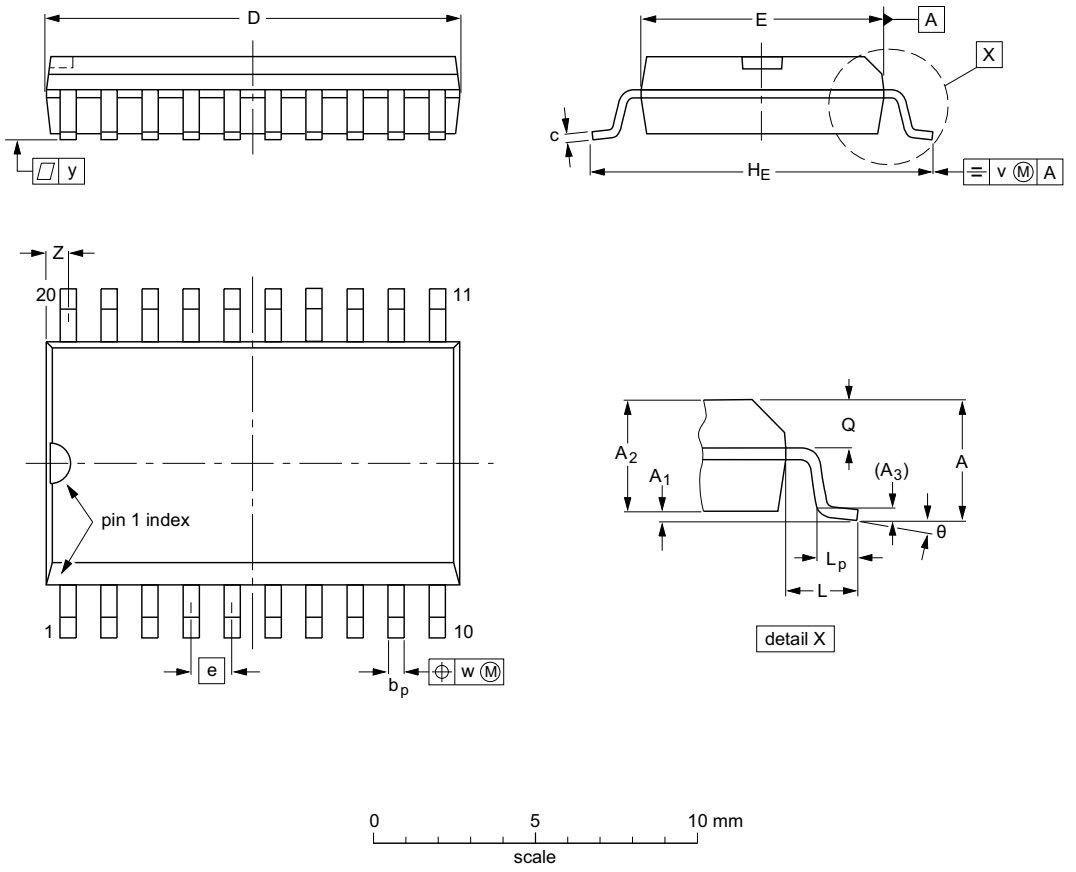
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT146-1		MS-001	SC-603			~~99-12-27~~ 03-02-13

Fig 8. Package outline SOT146-1 (DIP20)

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

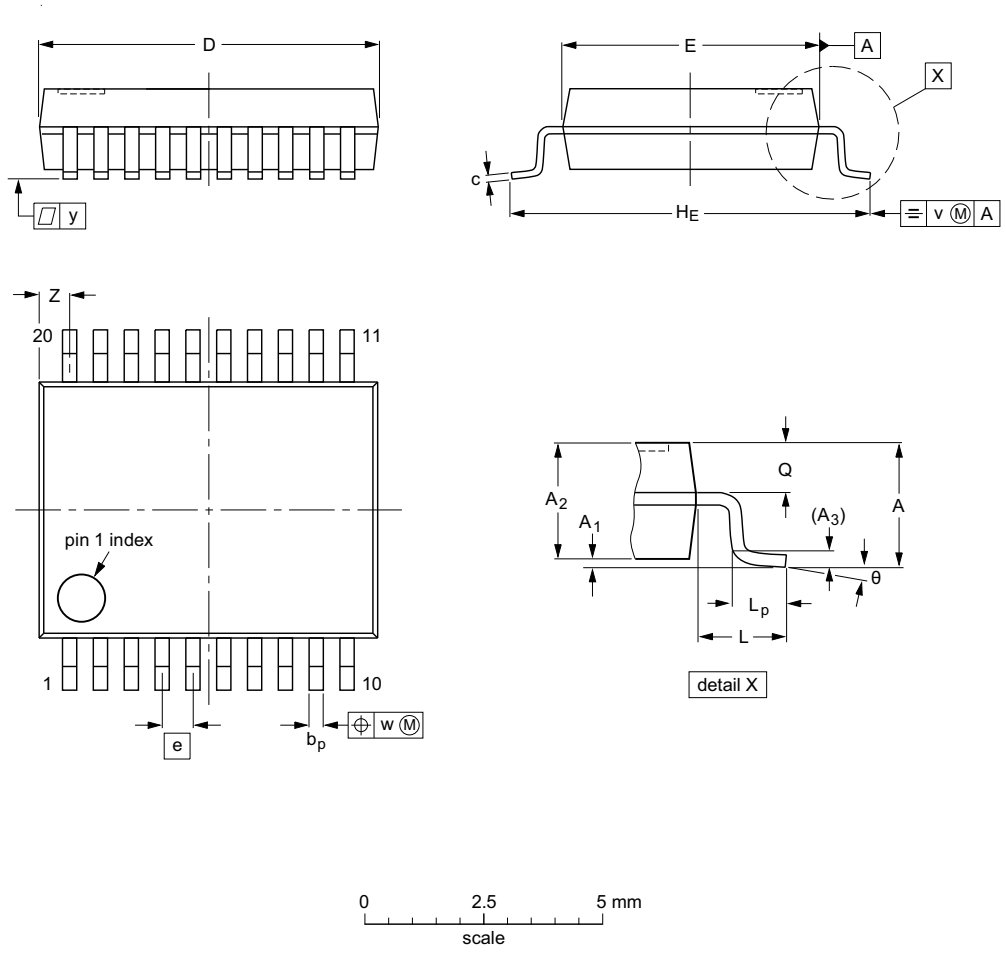
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8^o 0^o

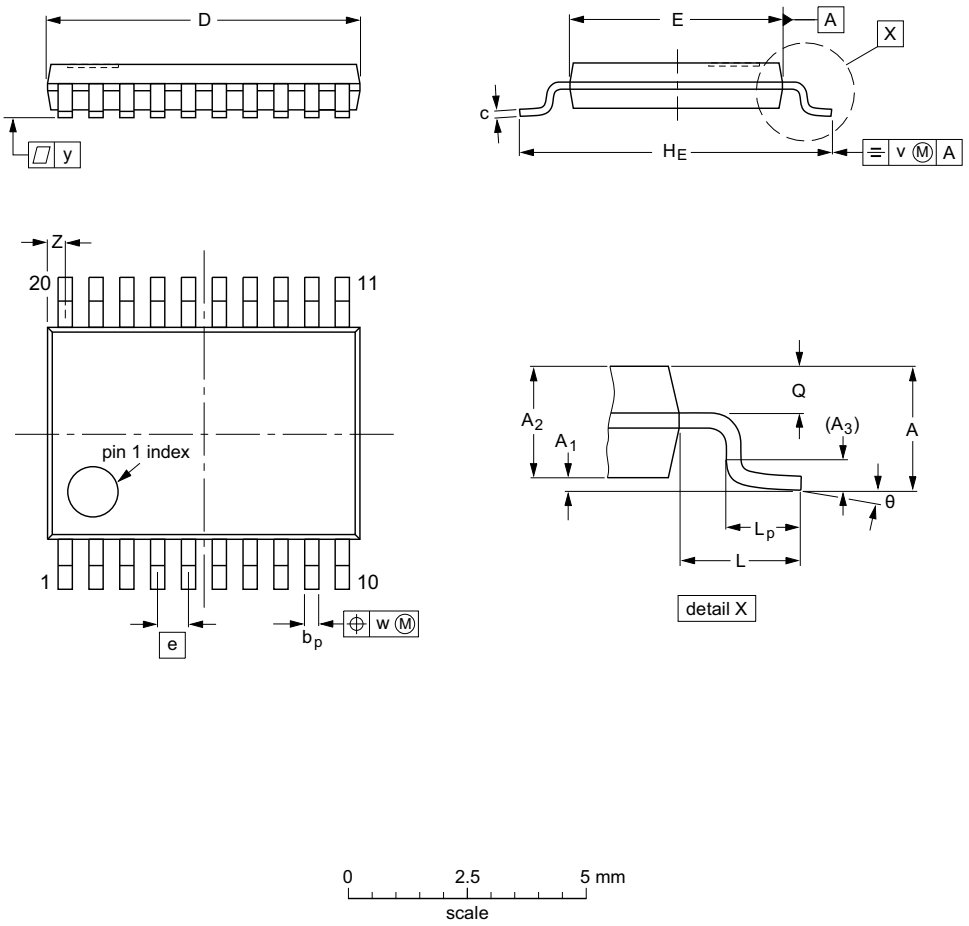
Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT360-1 (TSSOP20)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV244 v.3	20140311	Product data sheet	-	74LV244 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
74LV244 v.2	19980520	Product specification	-	74LV244 v.1
74LV244 v.1	-	-	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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16. Contact information

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For sales office addresses, please send an email to: **salesaddresses@nxp.com**

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Date of release: 11 March 2014
Document identifier: 74LV244